What is claimed is:

1. An internal voltage generating circuit in a semiconductor memory device, comprising:

a comparing means for comparing a voltage level of an internal voltage with that of a reference voltage;

a pull-up driving means for performing a pull-up operation for an output terminal in response to an output signal of the comparing means; and

a discharging means for discharging the output terminal in a period of which the voltage level of the internal voltage is higher than a predetermined target voltage level.

2. The internal voltage generating circuit as recited in claim 1, wherein the discharge means includes:

a first discharge unit for discharging the output terminal when the voltage level of the internal voltage is higher than a predetermined target voltage level in response to the internal voltage; and

a second discharge unit for discharging the output terminal in response to the power supply voltage.

3. An internal voltage generating circuit in a semiconductor memory device, comprising:

a comparing means for comparing a voltage level of an internal voltage with that of a reference voltage;

a pull-up driving means for performing a pull-up

operation for an output terminal in response to an output signal of the comparing means; and

a first discharging means for discharging the output terminal when the voltage level of the internal voltage is higher than a predetermined target voltage level in response to the internal voltage.

4. The internal voltage generating circuit as recited in claim 3, further comprising a second discharging means for discharging the output terminal in response to the power supply voltage.

5. The internal voltage generating circuit as recited in claim 3, wherein the first discharging means includes a plurality of active loads connected between the output terminal and a ground voltage in series.

6. The internal voltage generating circuit as recited in claim 5, wherein the first discharging means includes a plurality of diode-coupled NMOS transistor connected between the output terminal and a ground voltage in series

7. The internal voltage generating circuit as recited in claim 4, wherein the second discharge unit includes:

a voltage divider for producing a discharge control signal by dividing the power supply voltage; and

a discharge driver for performing a discharge operation

of the output terminal in response to the discharge control signal.

8. The internal voltage generating circuit as recited in claim 7, wherein the voltage divider includes first and second resistors connected between the power supply voltage and the ground voltage in series.

9. The internal voltage generating circuit as recited in claim 8, wherein the discharge driver includes an NMOS transistor which is connected between the output terminal and the ground voltage and whose gate receives the discharge control signal.

10. The internal voltage generating circuit as recited in claim 3, wherein the pull-up driving means includes a PMOS transistor which is connected between the power supply voltage and the output terminal and whose gate receives the output signal of the comparing means.